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Design and Simulation of Cascaded Multi Level Inverter with Less Number of Switches Fed Induction Motor Drive

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Abstract : *A new approach of 31-levels cascaded H-bridgemultilevel inverter is proposed for three phase induction motor drives. Power quality is improved with the increase in number of levels. However, the number of switching devices and other components increase which would result in increase in cost and control complexity. In this topology, only one bidirectional switch is employed for each transformer. However, in conventional cascaded transformer multilevel inverter, four switching devices are required for each transformer. Therefore, more output voltage levels can be obtained using fewer switching components. Reduction in the number of switching devices which also means reduction in the number of gate drivers results in smaller size and low implementation cost. Due to that, the switching loss gets reduced as same like the harmonic distortion occurs in the motor drive gets reduced. Also, it generally regularizes the stair –case voltage waveform from several dc sources which has reduced harmonic content. To mitigate this problem, we propose an efficient switching method for the prior H-bridge based multilevel inverter. The operation and performance of the proposed a three-phase 31-level inverter fed with induction motor drive is verified by MATLAB/ SIMULINK.*

Keywords - *Cascaded Multilevel Inverter developed H-bridge Multilevel Inverter, Voltage Source Inverterand Induction Motor.*

I. INTRODUCTION

Multilevel inverter has become more famous over previous years in high power electric applications without the usage of a transformer and filters [1]. Multilevel inverters can be categorized into three topologies, they are, diode-clamped, flying-capacitor and cascaded H-bridge cell. The idea of cascaded multilevel inverter is based on linking H-bridge inverters in series to attain an output of sinusoidal voltage. The output voltage is the sum of the voltage that is produced by each cell. As the number of levels gets increases, the synthesized output waveform has several steps which generate a staircase wave that approaches a preferred waveform [2]. The inverter source voltage generate an output voltage or a current among certain levels either 0 or ±Vdc is called as two-level inverter. Along with that, cascaded H-bridge multilevel inverters have been received an immense attention because of their qualities such as minimum number of components, reliability and modularity. In the point of view, attaining a sinusoidal output voltage wave, multilevel inverters may well increase the number of output voltage levels. Though, it will require more components resulted in complication and cost increase. This paper focuses on the transistor clamped H-bridge based multilevel inverter topology. Generally, among these topologies, the cascaded multilevel inverter has the possible to be the most reliable and achieve the best fault tolerance owing to its modularity; a feature that enables the inverter to continue operating at lower power levels after cell failure [3]. Modularity also permits the cascaded multilevel inverter to be stacked easily for high-power and high voltage applications. The concept of multilevel converters has been introduced since 1975. The cascade multilevel inverter was first proposed in 1975 [4]. Separate DC-sourced full-bridge cells are placed in series to synthesize a staircase AC output voltage. The term multilevel began with the three-level converter [5]. Subsequently, several multilevel converter topologies have been developed [6]. In 1981, diode-clamped multilevel inverter also called the Neutral Point Clamped (NPC) inverter schemes were proposed [7].

In 1992, capacitor-clamped (or flying capacitor) multilevel inverters, [8] and in 1996, cascaded multilevel inverters were proposed [9]. Although the cascade multilevel inverter was invented earlier, its application did not prevail until the mid-1990s. The advantages of cascade multilevel inverters were prominent for motor drives and utility applications. The cascade inverter has drawn great interest due to the great demand of medium-voltage high-power inverters. The cascade inverter is also used in regenerative-type motor drive applications

[10]. Recently, some new topologies of multilevel inverters have emerged. This includes generalized multilevel inverters [11], mixed multilevel inverters, hybrid multilevel inverters [12] and soft-switched multilevel inverters [13]. These multilevel inverters can extend rated inverter voltage and power by increasing the number of voltage levels. They can also increase equivalent switching frequency without the increase of actual switching frequency, thus reducing ripple component of inverter output voltage and electromagnetic interference effects. As the multilevel converter is broadly applied in the industries because the demand to operate switching, power converters in high power application has the growth constantly. The capacity of multilevel converters to operate at high voltages of the AC waveforms has low distortion, high quality and high efficiency. However, the multilevel converter [14] topology has improved efficiency by using various controls to attain high efficiency and increase to save energy. In this paper, the topology proposed is three phase 31-level cascaded multilevel H bridge inverter for three phase induction motor. A 31 level cascaded multilevel H bridge inverter to reduce the Total Harmonic Distortion (THD) [15] of the inverter output voltages for three-phase induction motor drive are presented.

II. PROPOSED TOPOLGY

In Fig.1, two new topologies are proposed for a seven-level inverter. As shown in. 1, the proposed topologies are obtained by adding two unidirectional power switches and one dc voltage source to the H-bridge inverter structure. In other words, the proposed inverters are comprised of six untidier tonal power switches (Sa, Sb, SL,1, SL,2, SR,1, and SR,2) an two dc voltage sources (VL,1 andVR,1). In this paper, these topologies are called developed H-bridge. As shown in Fig.1, the simultaneous turn-on of SL,1 and SL,2(orSR,1and SR,2)

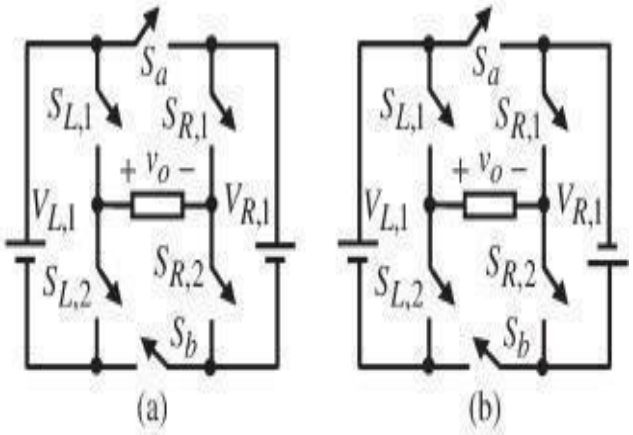

Fig.1. Proposed Seven-Level Inverters. (a) First Proposed Topology. (b) Second Proposed Topology.

Causes the voltage sources to short-circuit. Therefore, the simultaneous turn-on of the mentioned switches must be avoided. In addition, Sa and Sb should not turn on, simultaneously. The difference in the topologies illustrated in Fig.1 is in the connection of the dc voltage sources polarity. Table I shows the output voltages of the proposed inverters for different states of the switches. In this table, 1 and 0 indicate the ON- and OFF-states of the switches, respectively. As it is obvious from Table I, if the values of the dc voltage sources are equal, the number of voltage levels decreases to three. Therefore, the values of dc voltage sources should be different to generate more voltage levels without increasing the number of switches and dc voltage sources. Considering Table I, to generate all voltage levels (odd and even) in the proposed topology shown in Fig.1(a), the magnitudes of $V_{L,1}$ and $V_{R,1}$ should be considered 3puand 1pu, respectively. Similarly, for the topology shown in Fig.1 (a), the magnitudes of V_L, 1and$V_{R,\ 1}$ should be considered 2pu and 1pu, respectively. Considering the aforementioned explanations, the total cost of the proposed topology in Fig.1(b) is low because dc voltage sources with low magnitudes are needed. By developing the seven-level inverter shown in Fig.1 (b), the 31-level inverter shown in Fig.2 can be proposed. This topology consists of ten unidirectional power switches and four dc voltage sources. According to Fig. 2,if the power switches of ($S_{L,1}$,$S_{L,2}$), ($S_{L,3}$,$S_{L,4}$), ($S_{R,1}$,$S_{R,2}$), and ($S_{R,3}$,$S_{R,4}$)turn on simultaneously, the dc voltage sources of $V_{L,1}$, $V_{L,2}$, $V_{R,1}$, and $V_{R,2}$ will be short-circuited, respectively. Therefore, the simultaneous turn-on of these switches should be avoided. In addition, Sa and Sb should not turn on simultaneously. It is important to note that the 31-level topology can be provided through the structure presented in Fig.1(a), where the only difference will be in the polarity of the applied dc voltage sources. By eveloping the proposed 31-level inverter. This topology

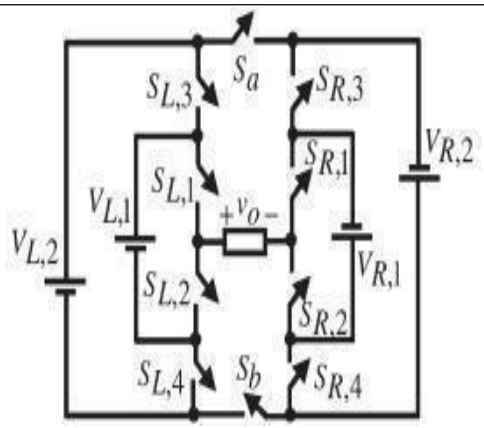

Fig.2. Proposed 31-Level Inverter

$$N_{\text{step}} = 2^{2n+1} - 1 \quad (1)$$

$$N_{\text{switch}} = 4n + 2 \quad (2)$$

$$N_{\text{source}} = 2n \quad (3)$$

$$V_{o,\max} = V_{L,n} + V_{R,n} \quad (4)$$

The other important parameters of the total cost of a multilevel inverter for evaluation are the variety of the values of dc voltage sources and the value of the blocking voltage of the switches. As the variety of dc voltage sources and the value of the blocking voltage of the switches are low, the inverter's total cost decreases [2]. The number of variety of the values of dc voltage sources (Variety) is given by

$$N_{\text{variety}} = 2n$$

The following pattern is utilized to calculate the maximum Magnitude of the blocking voltage of the power switches. As shown in Fig.1 (b), the blocking voltage of SR, 1and SR, 2 is calculated as follows:

$$V_{\text{SR},1} = V_{\text{SR},2} = V_{R,1} \quad (6)$$

WhereVSR, 1 andVSR, 2 indicate the maximum blocking voltages ofSR, 1andSR,2, respectively. The blocking voltage of SL, 1andSL, 2are as follows

$$V_{\text{SL},1} = V_{\text{SL},2} = V_{L,1} \quad (7)$$

Where VSL, 1andVSL, 2indicate the maximum blocking voltages of SL, 1andSL, 2, respectively. Therefore, the maximum blocking voltage of all switches in the proposed seven-level inverter (Vblock, 1) is calculated as follows

$$V_{\text{block},1} = V_{\text{SR},1} + V_{\text{SR},2} + V_{\text{SL},1} + V_{\text{SL},2} + V_{Sa} + V_{Sa}$$

$$= 4(V_{R,1} + V_{L,1}). \quad (8)$$

Considering Fig.2, the maximum blocking voltage of the switches is as follows:

$$V_{SR,1} = V_{SR,2} = V_{R,1} \quad 9)$$

$$V_{SR,3} = V_{SR,4} = V_{R,2} - V_{R,1} \quad 10)$$

$$V_{SL,1} = V_{SL,2} = V_{L,1} \quad 11)$$

$$V_{SL,3} = V_{SL,4} = V_{L,2} - V_{L,1} \quad (12)$$

$$V_{Sa} = V_{Sb} = V_{R,2} + V_{L,2} \quad (13)$$

Therefore, the maximum blocking voltage of all switches of the proposed 31-level inverter (Vblock, 2) is as follows

$$V_{block,2} = V_{SR,1} + V_{SR,2} + V_{SR,3} + V_{SR,4} + V_{SL,1} + V_{SL,2} + V_{SL,3} + V_{SL,4} + V_{Sa} + V_{Sb} = 4(V_{R,2} + V_{L,2}). \quad (14)$$

Similarly, the maximum blocking voltage of all switches of the 127-level inverter is calculated as follow:

$$V_{block,3} = 4(V_{R,3} + V_{L,3}) \quad (15)$$

Finally, the maximum blocking voltage of all the switches of the general topology (Vblock, n) is calculated as follows:

$$V_{block,n} = 4(V_{R,n} + V_{L,n}) \quad (16)$$

III. PERFORMANCE OF THE INDUCTIONMOTOR

The sinusoidally-distributed flux density wave produced by the stator magnetizing currents sweeps past the rotor conductors, it generates a voltage in them. The result is a sinusoidally-distributed set of currents in the short-circuited rotor bars.Because of the low resistance of these shorted bars, only a small relative angular velocity, r, between the angular velocity, s, of the flux wave and the mechanical angular velocity of the two-pole rotor is required to produce the necessary rotor current.The relative angular velocity, r, is called the slip velocity.The interaction of the sinusoidally -distributed air gap flux density and induced rotor currents produces a torque on the rotor. The typical induction motor speed-torque characteristic

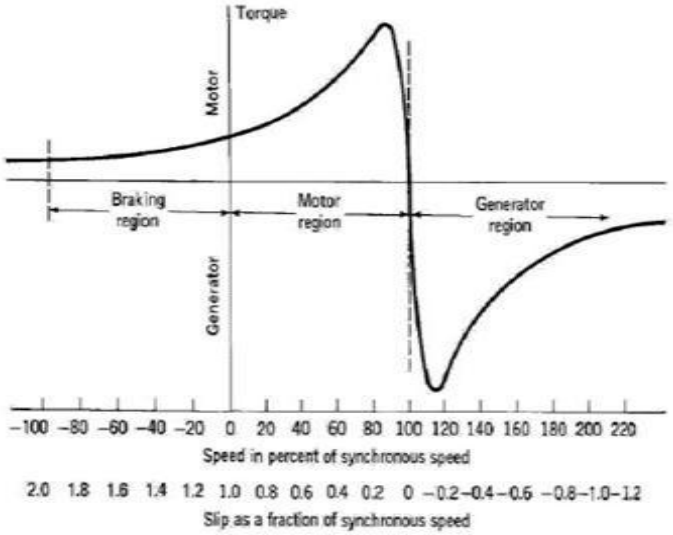

Fig.3. Speed-Torque Characteristics of Induction Motor. an Induction Motor (IM) is a Type of Asynchronous ACMotor Where Power is Supplied to the Rotating Device

By Means of Electromagnetic Induction. An Electric Motor Convert's Electrical Power to Mechanical Power in its Rotor. There are Several Ways to Supply Power to the Rotor. In a DC Motor this Power is Supplied to the Armature Directly from a DC Source, While in an Induction Motor This Power is Induced in the Rotating Device. An Induction Motor is Sometimes Called a Rotating Transformer Because the Stator (Stationary Part) is Essentially the Primary Side of the Transformer and the Rotor (Rotating Part) is the Secondary Side. Induction Motors are Widely Used, Especially Poly Phase Induction Motors, Which are Frequently Used in Industrial Drives. When Induction Motors are Given Supply, They Draw the Current As

$$Ia = \frac{\quad}{\quad} \quad \text{As initially } Eb = 0 \qquad (17)$$

Motor draws a very high current initially; due to which voltage dip will forms, which show the effect on the power system network. In order to avoid such problems a effective controlled APF is placed without effecting the power quality or the motor performance characteristics.

IV. FIGURES AND TABLES

TABLE I. Output Voltages of the Proposed Seven-Level Inverters

No.	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_a	S_b	v_o (Fig. 1(a))	v_o (Fig. 1(b))
1	1	0	0	1	0	1	$V_{L,1}$	$V_{L,1}$
2	1	0	0	1	1	0	$V_{R,1}$	$-V_{R,1}$
3	1	0	1	0	0	1	$V_{L,1}-V_{R,1}$	$V_{L,1}+V_{R,1}$
4	1	0	1	0	1	0	0	0
	0	1	0	1	0	1		
5	0	1	1	0	1	0	$-V_{L,1}$	$-V_{L,1}$
6	0	1	1	0	0	1	$-V_{R,1}$	$V_{R,1}$
7	0	1	0	1	1	0	$-(V_{L,1}-V_{R,1})$	$-(V_{L,1}+V_{R,1})$

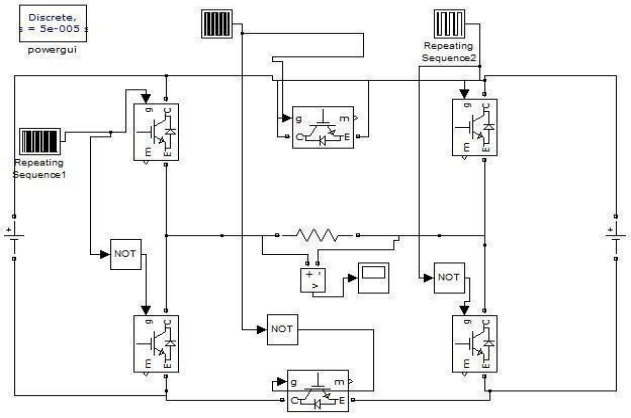

Fig.4.Simulink Circuit for Seven Level Inverter.

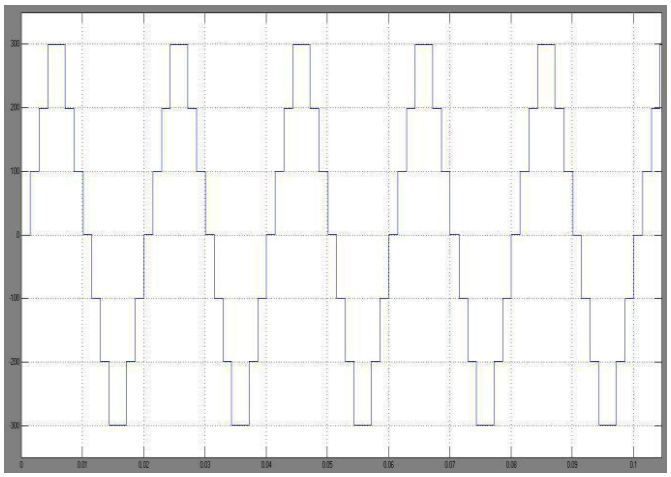

Fig.5. Simulation Results for Seven Level Inverter.

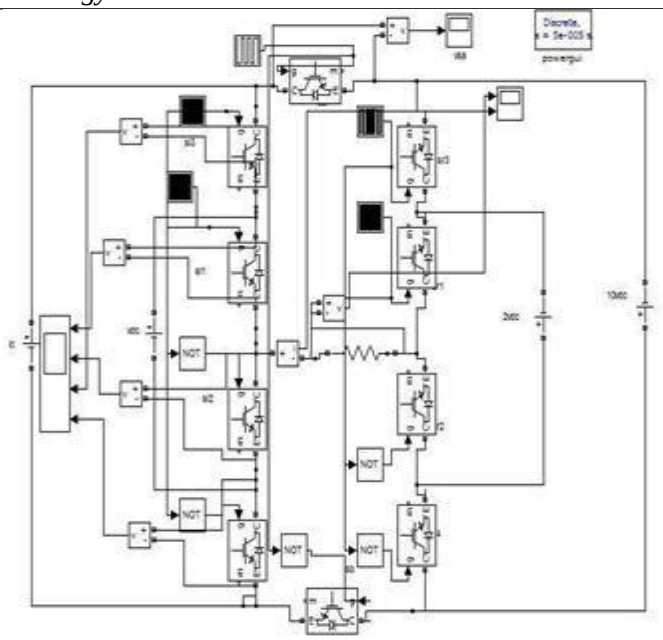

Fig.6. Simulation Results for 31 Level Inverter.

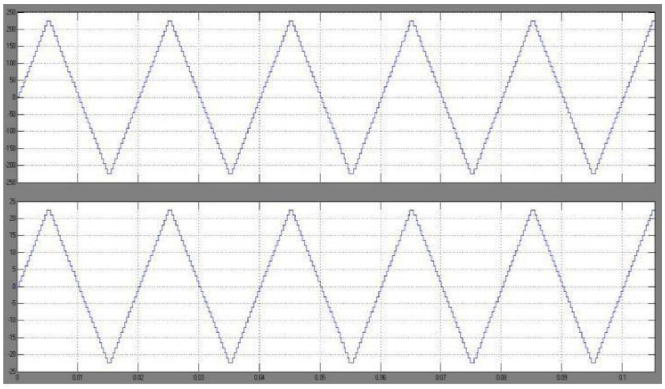

Fig.7. Simulation Results Voltage and Current for 31 Level Inverter.

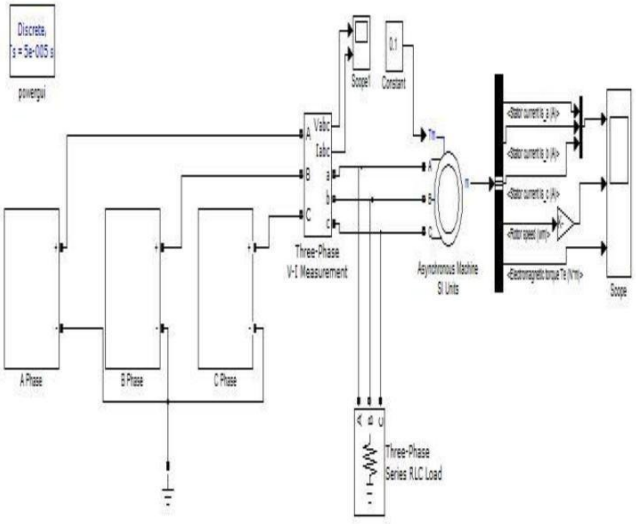

Fig.8. Simulink Circuit Induction Motor Fed 31 Level Inverter.

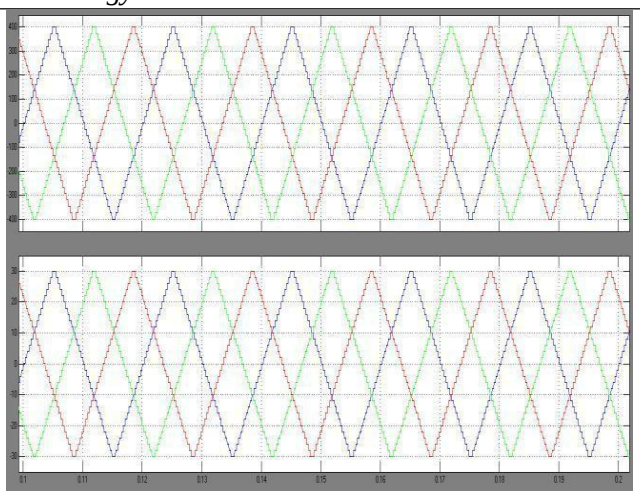

Fig.9. Simulation Results for Three Phase Voltage and Current.

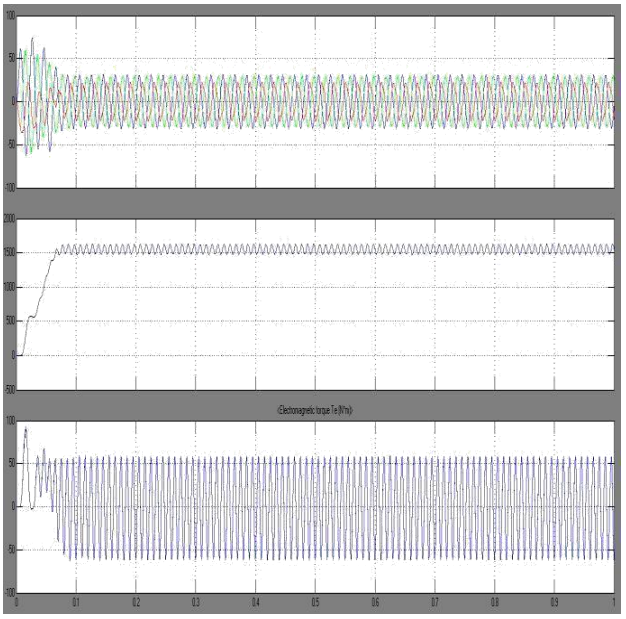

Fig.10. Simulation Results for Motor Characteristics

V. CONCLUSION

In this paper, a new inverter topology for induction motor drive has been proposed which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability. In this paper, two basic topologies have been proposed for multilevel inverters to generate seven voltage levels at the output. The basic topologies can be developed to any number of levels at the output where the 31-level and general topologies are consequently presented. In addition, a new algorithm to determine the magnitude of the dc voltage sources has-been proposed. The proposed general topology was compared with the different kinds of presented topologies in literature from different points of view. According to the comparison re salts, the proposed topology requires a lesser number of IGBTs, power diodes, driver circuits, and dc voltage sources. Moreover, the magnitude of the blocking voltage of the switches is lower than that of conventional topologies. However, the proposed topology has a higher number of varieties of dc voltage sources in comparison with the others. The proposed topology was verified through the Matlab/Simulink platform for 31-level inverter with induction motor drive**.**

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